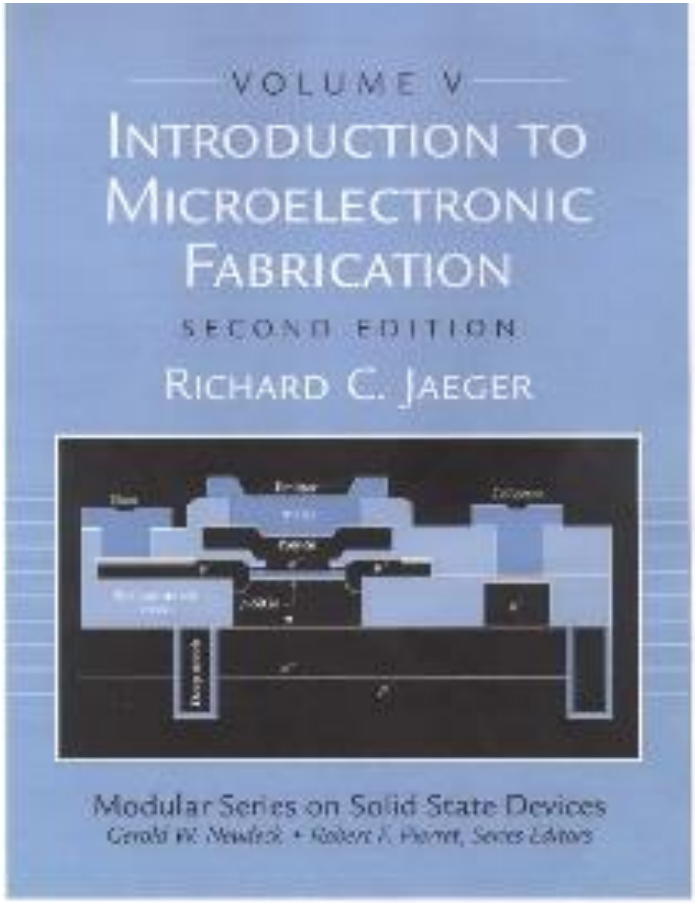
CMOS Manufacturing

- CMOS Manufacturing
  - Trends
  - Cost per transistor
- Process Flow
  - Nodes/Pitch/Feature size
  - Lithography Mask
  - Optical Proxmity Correction
  - Variability
- Specific Layout
  - Standard Cells
  - NAND/NOR
- Homework: Read Chapter 1 Jaeger



Historical Trends
Silicon Wafer Size

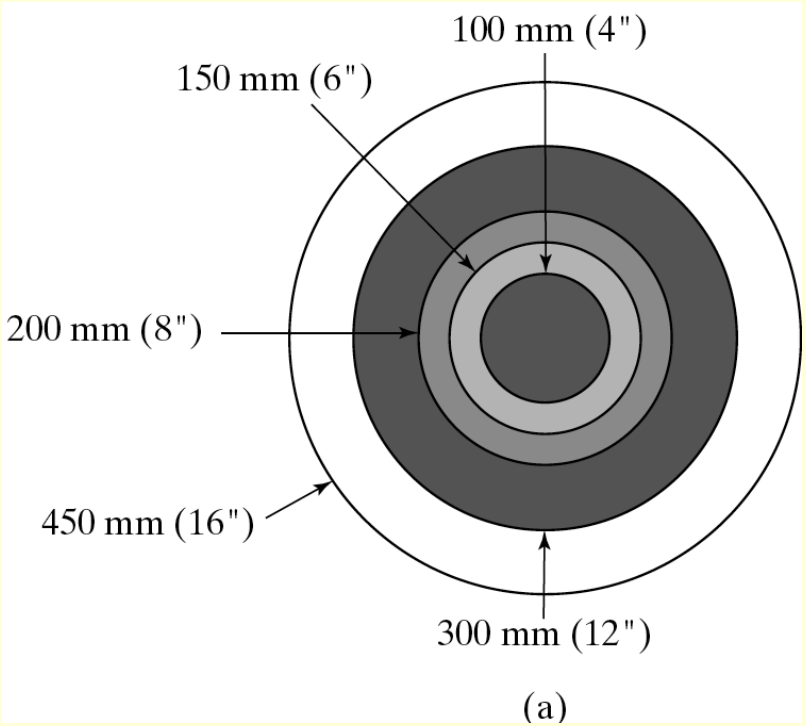


FIGURE 1.1

(a) Relative size of wafers with diameters ranging from 100 to 450 mm; (b) The same integrated circuit die is replicated hundreds of times on a typical silicon wafer; (c) the graph gives the approximate number of 10 x 10 mm dice that can be fabricated on wafers of different diameters.

- Early Wafers - 1, 1.5, 2 Inch Diameters
- Wafer Size has Increased Steadily
- 200 mm (8") Wafers in Production
- 300 mm (12") On Line Now (> 3B$/Fab)
- 450 mm Planned

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Modern CMOS Fabrication Plant

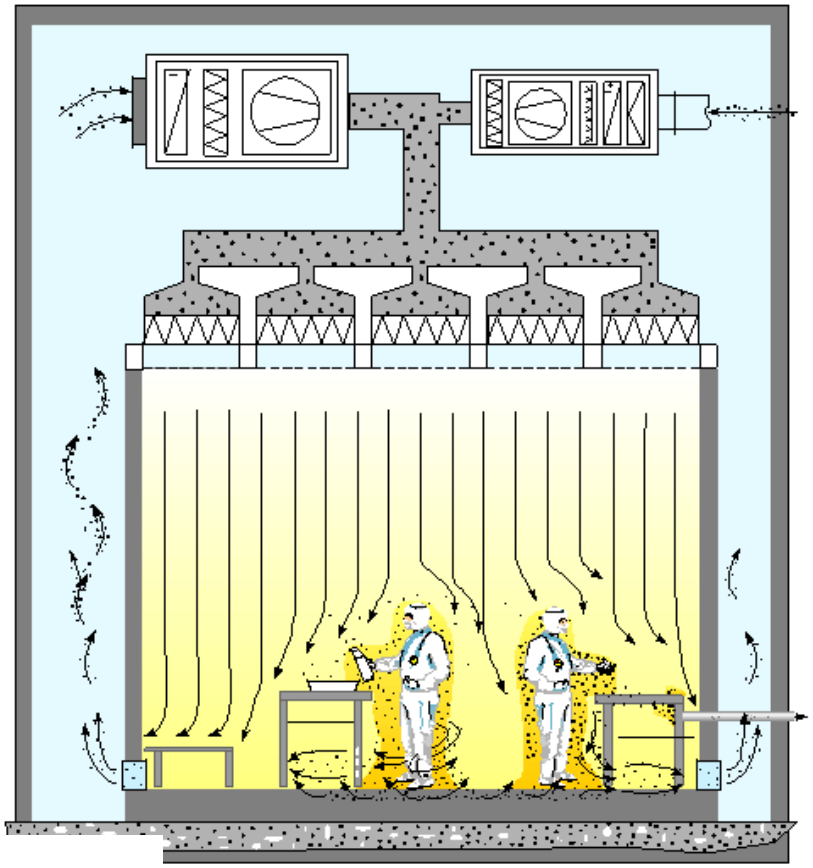
Intel engineer 300 mm wafer

- Inside of Intel/Micron 300mm NAND Memory Production Facility
  - One of many processing bays
- Buddy suit, air flow, overhead FOUP (25 wafers)
- Not a lot of engineers visible (highly automated)

http://www.pcworld.com/article/188459/inside_flash_memory_manufacturing.html

Clean Room Standards and HEPA Filters

- **H**igh **E**fficiency **P**articulate **A**ir (HEPA) filter
- **I**nternational **S**tandards **O**rganization(ISO)
- Cleanrooms classified by how clean the air is
- Ambient air ~ 35 million particles of size 0.5um (diameter) or larger in cubic meter
- ISO 1 clean room ~ 0



Source: en.wikipedia.org

ISO 14644-1 Cleanroom Standards

Class	maximum particles/m^3						FED STD 209E equivalent
	>=0.1 µm	>=0.2 µm	>=0.3 µm	>=0.5 µm	>=1 µm	>=5 µm	
ISO 1	10	2					
ISO 2	100	24	10	4			
ISO 3	1,000	237	102	35	8		Class 1
ISO 4	10,000	2,370	1,020	352	83		Class 10
ISO 5	100,000	23,700	10,200	3,520	832	29	Class 100
ISO 6	1,000,000	237,000	102,000	35,200	8,320	293	Class 1,000
ISO 7				352,000	83,200	2,930	Class 10,000
ISO 8				3,520,000	832,000	29,300	Class 100,000
ISO 9				35,200,000	8,320,000	293,000	Room Air

http://www.cleanairtechnology.com/cleanroom-classifications-class.php

Wafers: Front-End Unified Pod (or FOUP)

http://www.pcworld.com/article/188459/inside_flash_memory_manufacturing.html

- Unique areas in Fab for different types of process steps:
  - Photolithography, film deposition, etch, diffusion, ion implantation, chemical mechanical polish, etc.

Photolithography and Wet Bay

Lithography

Wet

http://www.pcworld.com/article/188459/inside_flash_memory_manufacturing.html

- Yellow light in photolithography bay to prevent unwanted exposure
- Linked photolithography track: spin, expose, develop

The Chase: (behind The Bay)

- Chemical, gases and power to tools
- Not as clean

Automated Wafer Handling System (AWHS)

- Industrial engineer design clean room track and scheduling system for automated movement of wafers from tool to tool
- Watch "*Semiconductor Technology at TSMC, 2011*"

  https://www.youtube.com/watch?v=4Q_n4vdyZzc

Industry Consortium Sets Wafer Handling Specifications

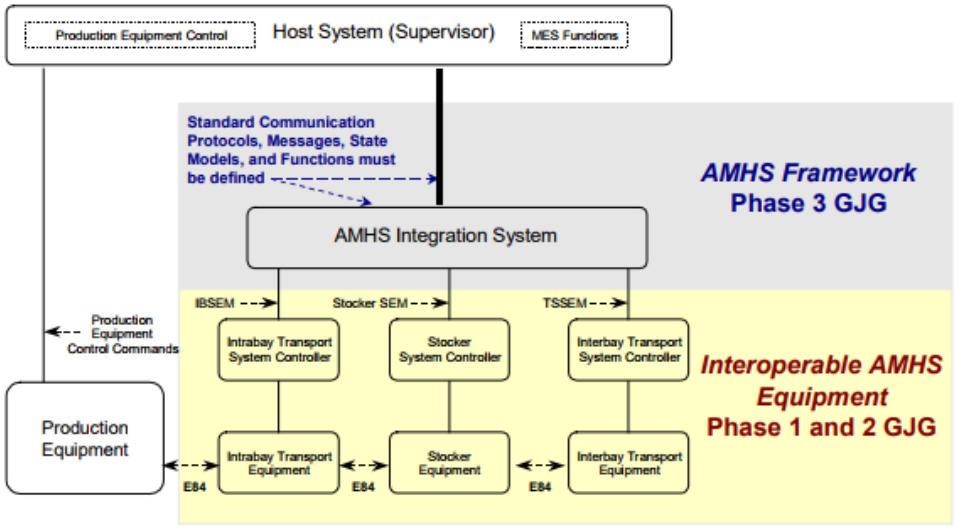


Figure 1 AMHS Framework

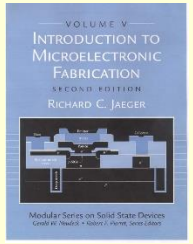
- Many industry associations to help **set standards** and **shared R&D**: SEMATECH, Semiconductor Industry Association(SIA), Semiconductor Research Corporation (SRC)

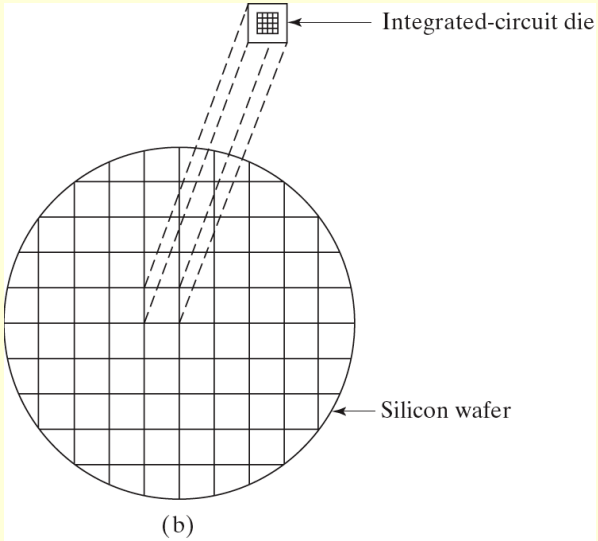
Manufacturing Plant Cost

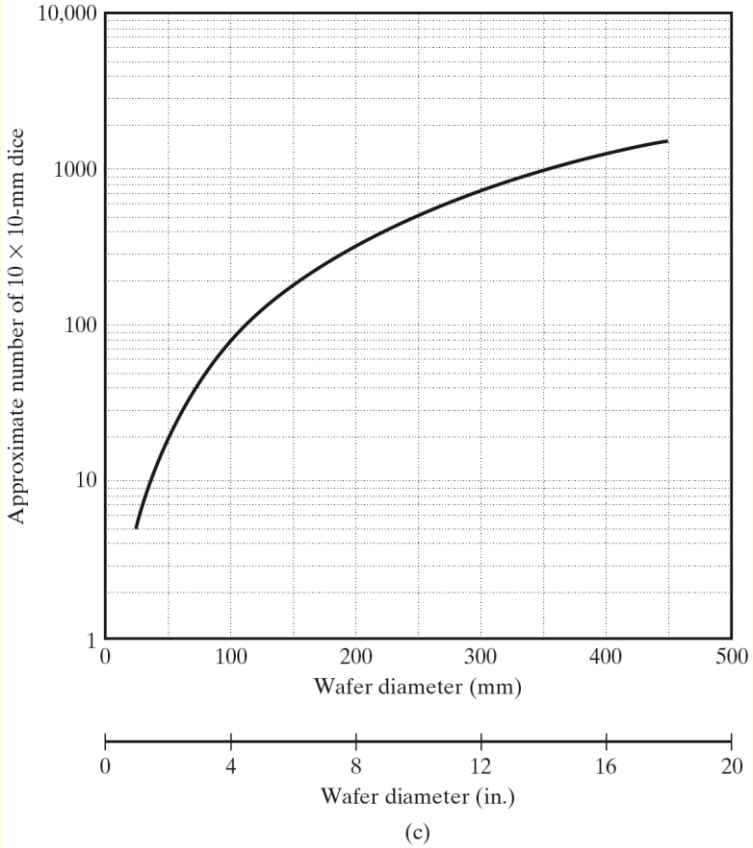
Intel's Estimated Fabrication Plant Cost

- Industry transitioned from (i) dedicated production lines to (ii) centralized production to (iii) merchant foundries (make chips for 10's to 100's of fabless semiconductor companies)

Larger Wafers
Lower Die Cost







- Cost to Process a Wafer is Relatively Fixed for a Given Process
- Larger Wafer →Lower Cost/Die

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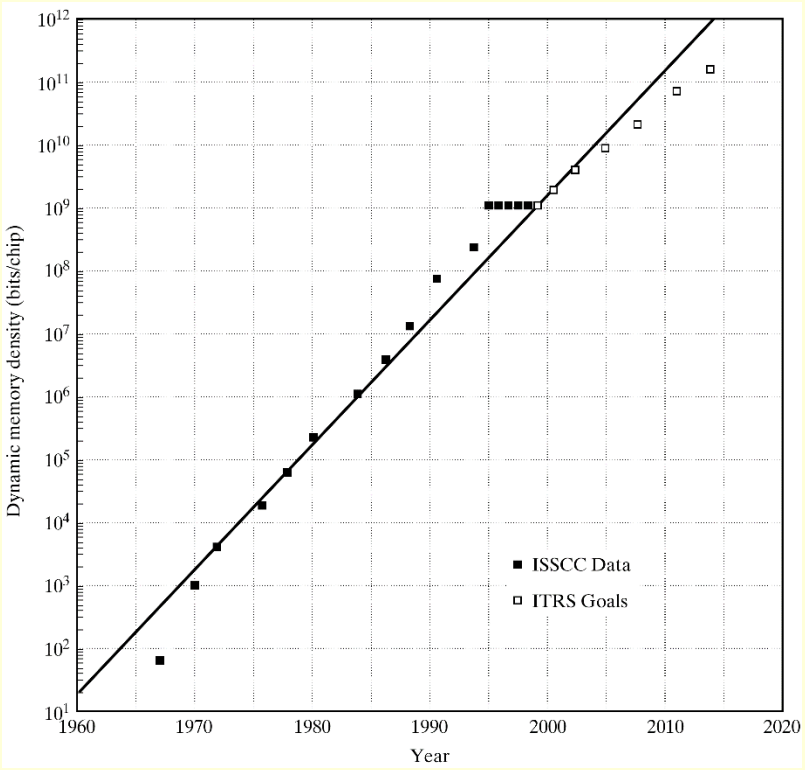
Historical Trends
Memory Density (Bits/Chip)



- Moore's Law - Exponential Increase in Chip Complexity
- ISSCC Research Benchmarks
  - 1967 - 64 bit Memory
  - 1984 - 1Mb Memory
  - 1995 - First 1 Gb Memory

FIGURE 1.2

(a) Dynamic memory density versus year since 1960.

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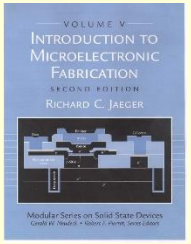
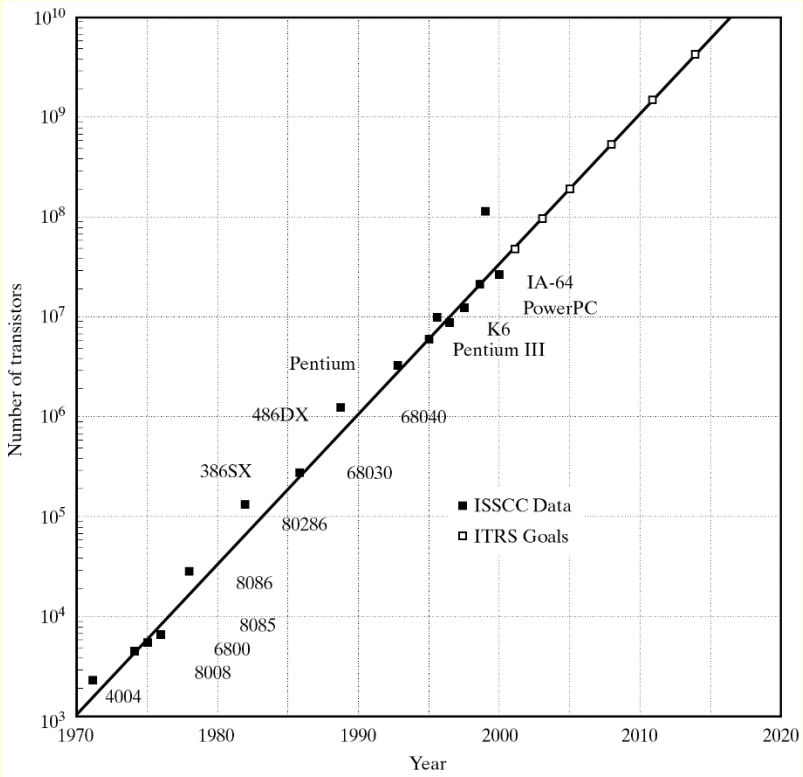
Historical Trends

Microprocessor Complexity (Trans./Chip)



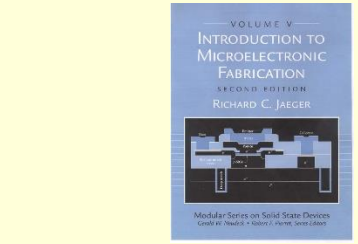


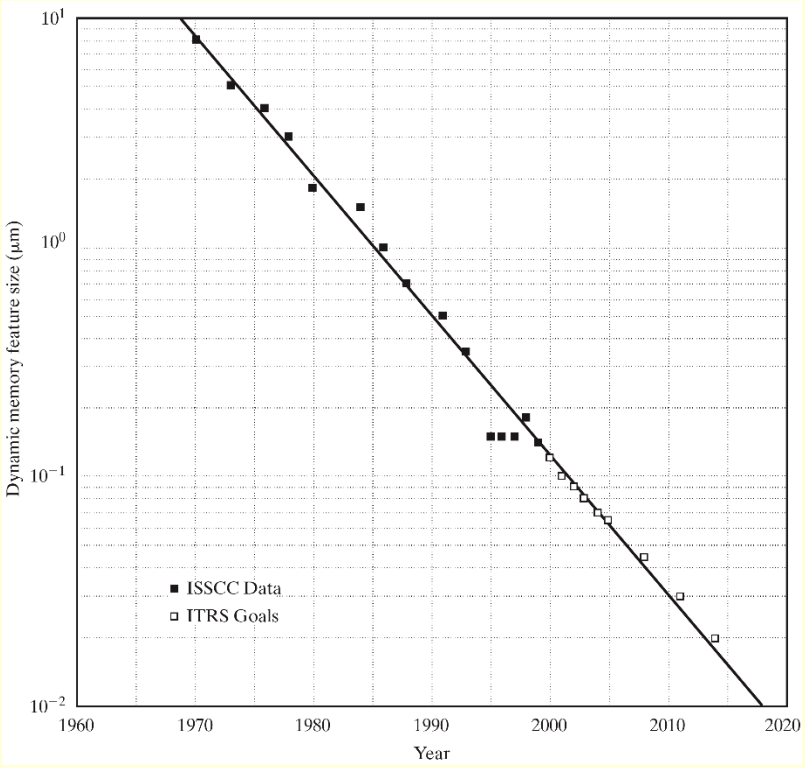
- ISSCC Benchmarks
  - 1971 - 2000 Transistors
  - 1988 - 1M Transistors
  - 1998 - 100M Transistors

FIGURE 1.2

(b) Number of transistors in a microprocessor versus year.

Historical Trends
Memory Feature Size (μm)





- Feature Size Decreases by 2X approximately every 5 years
- Each New Process Generation Doubles Density - Reduction of Feature Size by 0.707
- The Original Nanotechnology!
  - Feature size now 70-90 nm
- Transistors Operate Normally

FIGURE 1.3

Feature size used in fabrication of dynamic memory as a function of time.

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Homework: Watch ALL

- Watch "*Semiconductor Technology at TSMC, 2011*"

  https://www.youtube.com/watch?v=4Q_n4vdyZzc

- *"How Microchips Are Made"*
  - https://www.youtube.com/watch?v=F2KcZGwntgg
- GLOBALFOUNDRIES Sand to Silicon
  - https://www.youtube.com/watch?v=UvluuAIiA50
- Transistor Full Documentary
  - https://www.youtube.com/watch?v=U4XknGqr3Bo
    - History of invention from FET to point contact to BJT
    - Transistor: transfer resistor
    - Early products: radio (sony) and military
    - 1961 Integrated Circuit / Fairchild
    - Why field effect transistor NOT work
    - Point contact by accident/luck (opportunity meets prepared mind)
    - Few see vision of potential
    - Shockley/Bardeen/Brattain or Bell labs do not get rich of invention…Noyce/Moore do
    - Note dynamics of ego and team work
    - Note important of all type of smart people with different backgrounds for invention (theoretical and experimentalists from different fields)

Semiconductor Industry Roadmap - ITRS

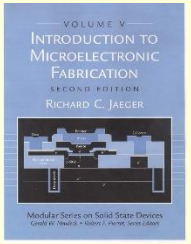


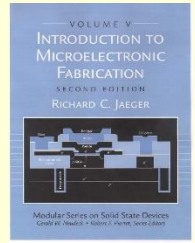
TABLE 1.1 International Technology Road Map for Semiconductors (ITRS) [4]

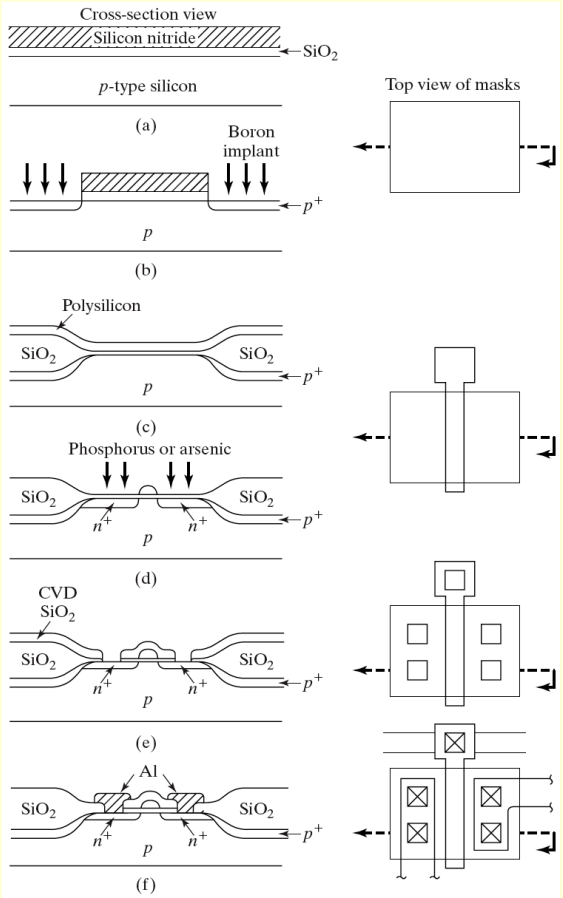
	Selected Projections					
Year of First Product Shipment	2001	2003	2005	2008	2011	2014
DRAM Metal Line Half-Pitch (nm)	150	120	100	70	50	35
Microprocessor Gate Widths (nm)	100	80	65	45	30	20
DRAM (G-bits/chip)	2.2	4.3	8.6	24	68	190
Microprocessor (M-transistors/chip)	48	95	190	540	1500	4300
DRAM Chip Area: Year of Introduction (mm^2)	400	480	526	600	690	790
DRAM Chip Area: Production (mm^2)	130	160	170	200	230	260
MPU Chip Size at Introduction (mm^2)	340	370	400	470	540	620
MPU Chip Area: Second "shrink" (mm^2)	180	210	230	270	310	350
Wafer Size (mm)	300	300	300	450	450	450

[4] *The International Technology Roadmap for Semiconductors*, The Semiconductor Industry Association (SIA), San Jose, CA, 1999. (http://www.semichips.org)

Each new process generation doubles chip density by scaling feature size by 0.7.

Basic NMOS Process
Key Steps

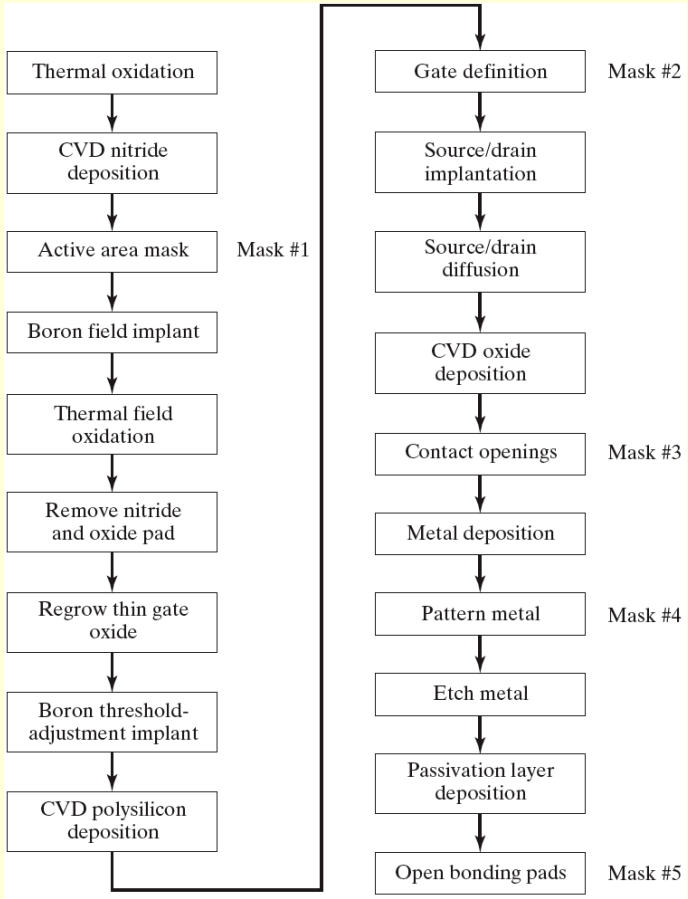




- Oxidation
- Photolithography
- Implantation
- Diffusion
- Etching
- Film Deposition

FIGURE 1.6

Process sequence for a semirecessed oxide NMOS process. (a) Silicon wafer covered with silicon nitride over a thin padding layer of silicon dioxide; (b) etched wafer after first mask step. A boron implant is used to help control field oxide threshold; (c) structure following oxidation, nitride removal, and polysilicon deposition; (d) wafer after second mask step and etching of polysilicon; (e) the third mask has been used to open contact windows following silicon dioxide deposition; (f) final structure following metal deposition and patterning with fourth mask.

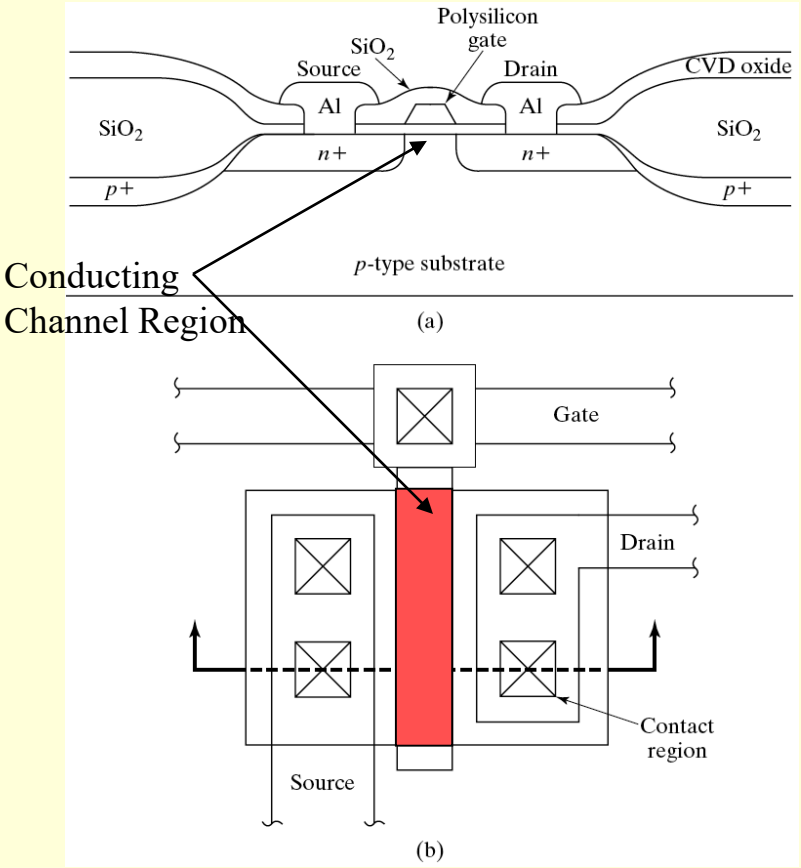


Simple CMOS Masking Steps

- Isolation
- N-well
- P-well
- Gate
- N type Source/drain extension
- P type source/drain extenstion
- N type source/drain
- P type source drain
- Contact
- Metal 1
- Via 1
- Metal 2
- ……. (repeat for additional metal layes ~10+)
- Top layer metal and packaging

NMOS Transistor

Top View and Cross-Section



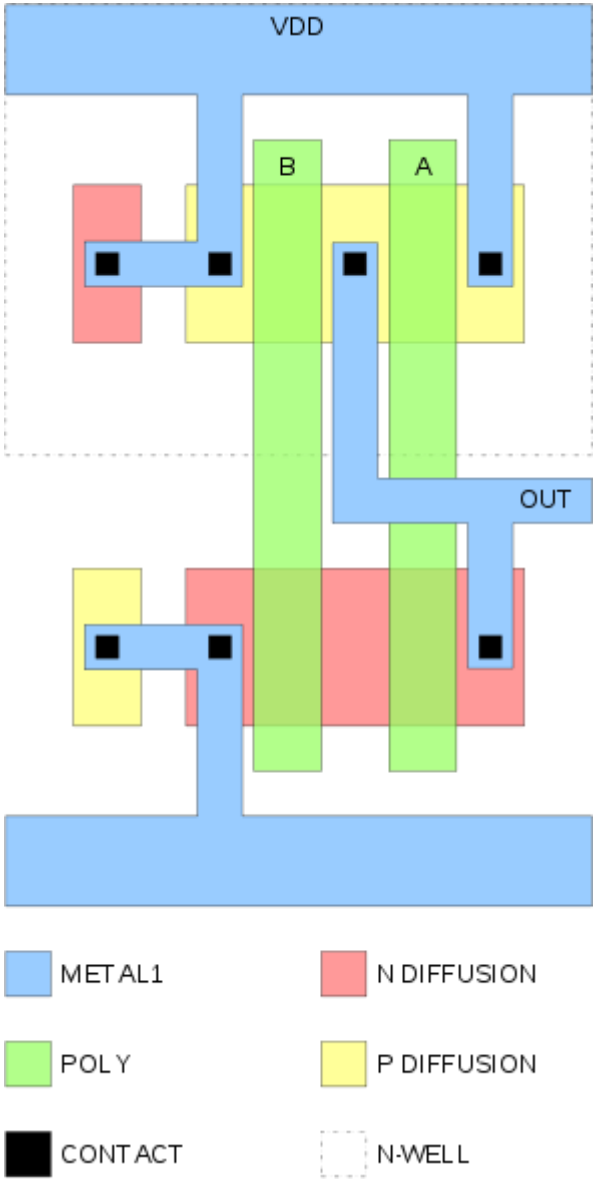
- N-Channel Metal-Oxide Semiconductor Transistor
- n- and p-type semiconductor regions
- Thick and thin oxides
- Etching Openings
- Polysilicon gate
- Metal (Al) Interconnections

FIGURE 1.4

The basic structure of an *n*-channel metal-oxide-semiconductor (NMOS) transistor structure. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a). The transistor uses heavily doped polysilicon as the gate "metal."

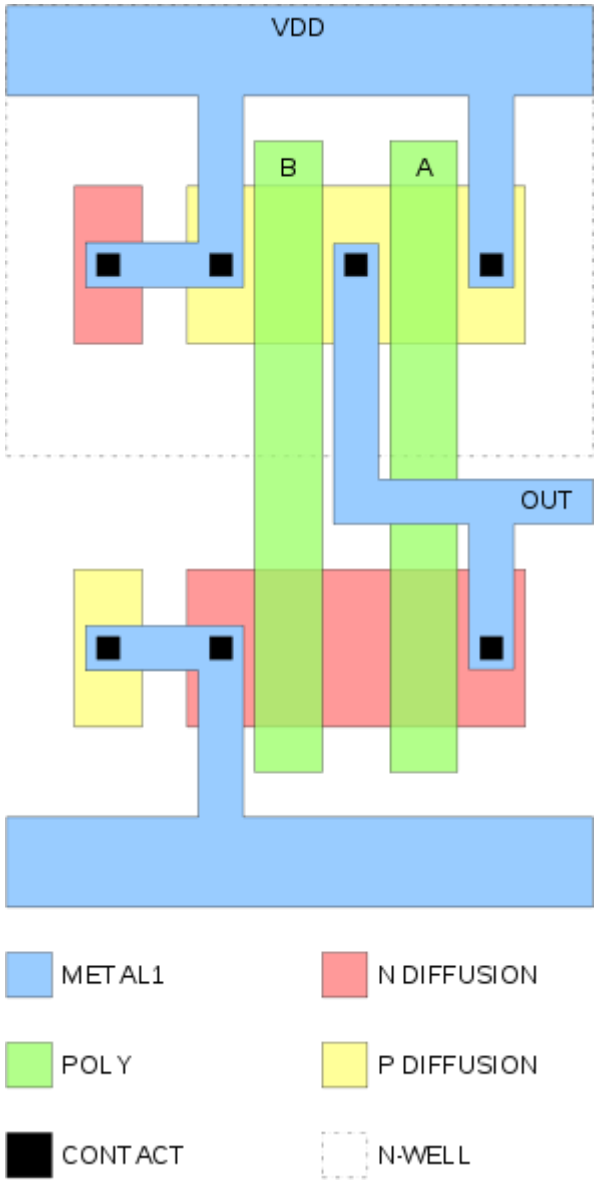
Layout of CMOS Inverter/NAND/NOR Gate

- Simple
- No Gate connects shown
- Note well contacts
- Can you draw Gate and Metal 1 Mask pattern
- Contact mask pattern
- N-Well

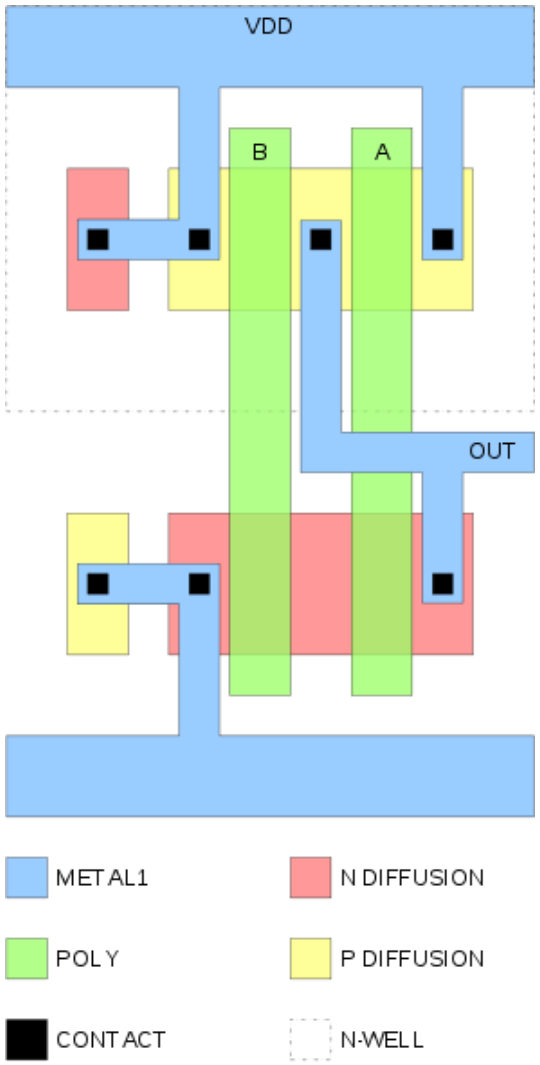


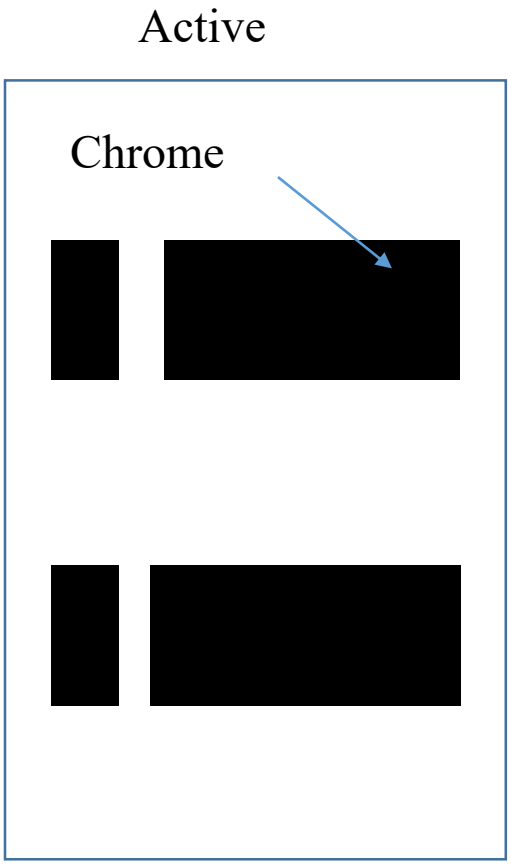
Source: wikimedia.org

Draw Isolation Mask



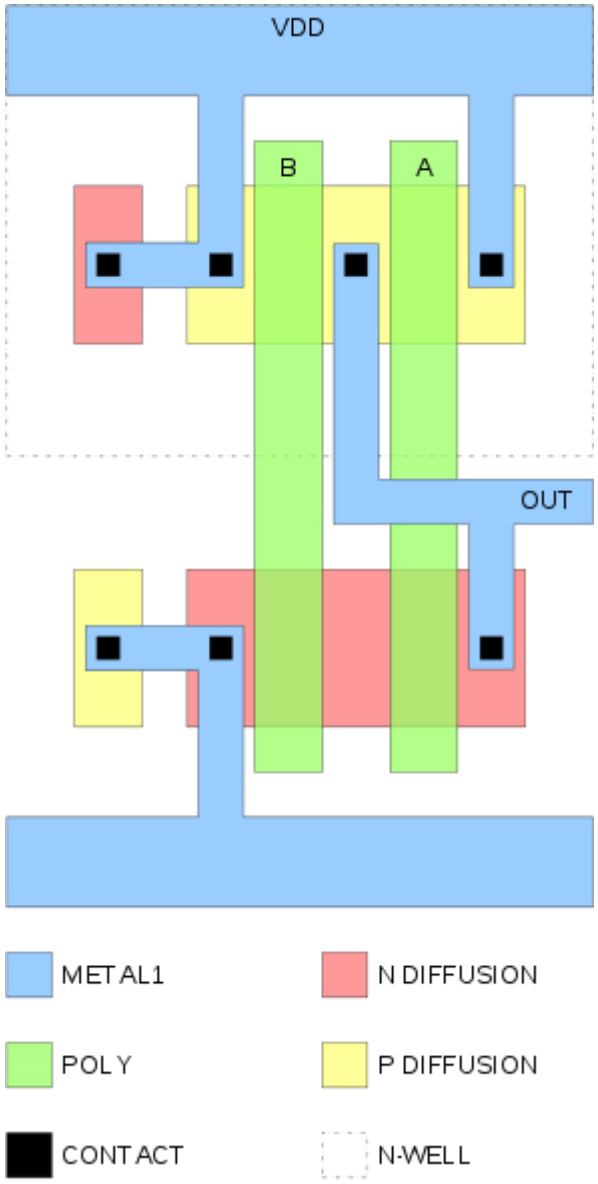
Solution Isolation Mask



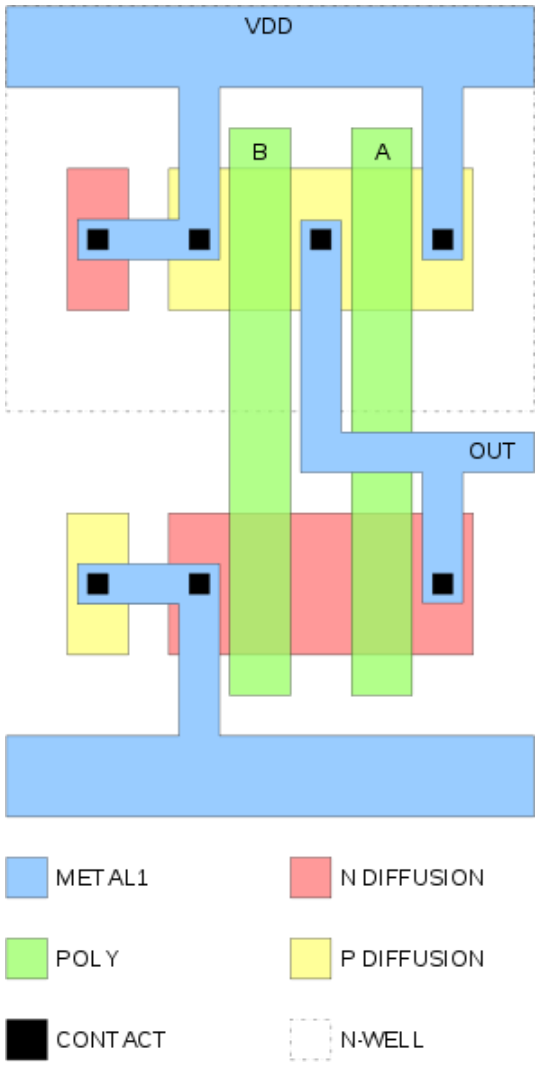


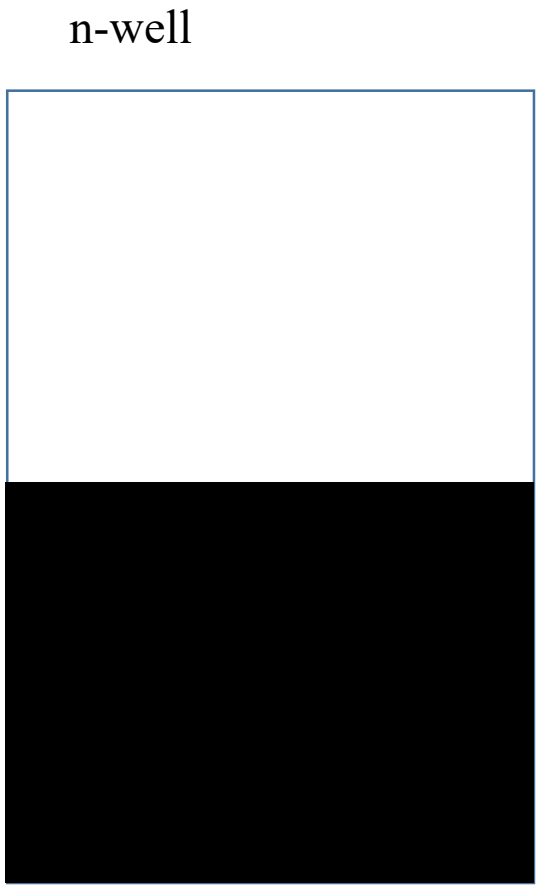
Can you draw process cross section cut?

Draw N-well Mask



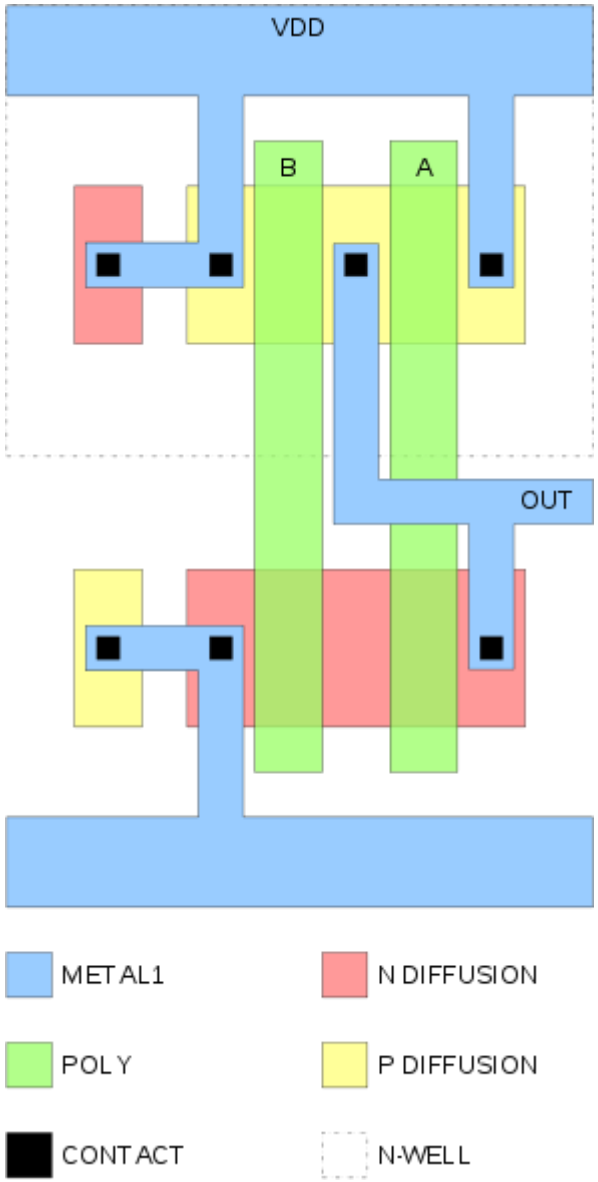
Solution N-well Mask



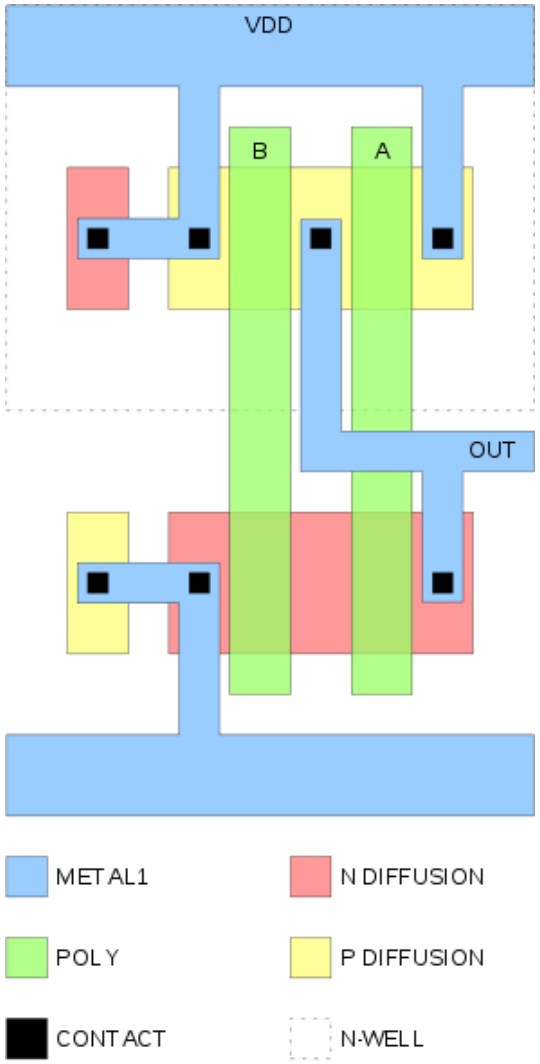


Can you draw process cross section cut?

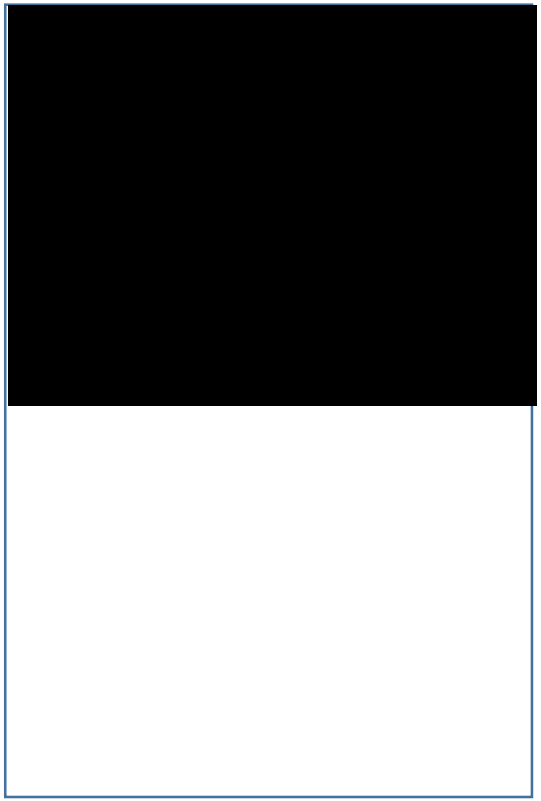
Draw P-well Mask



Solution P-well Mask



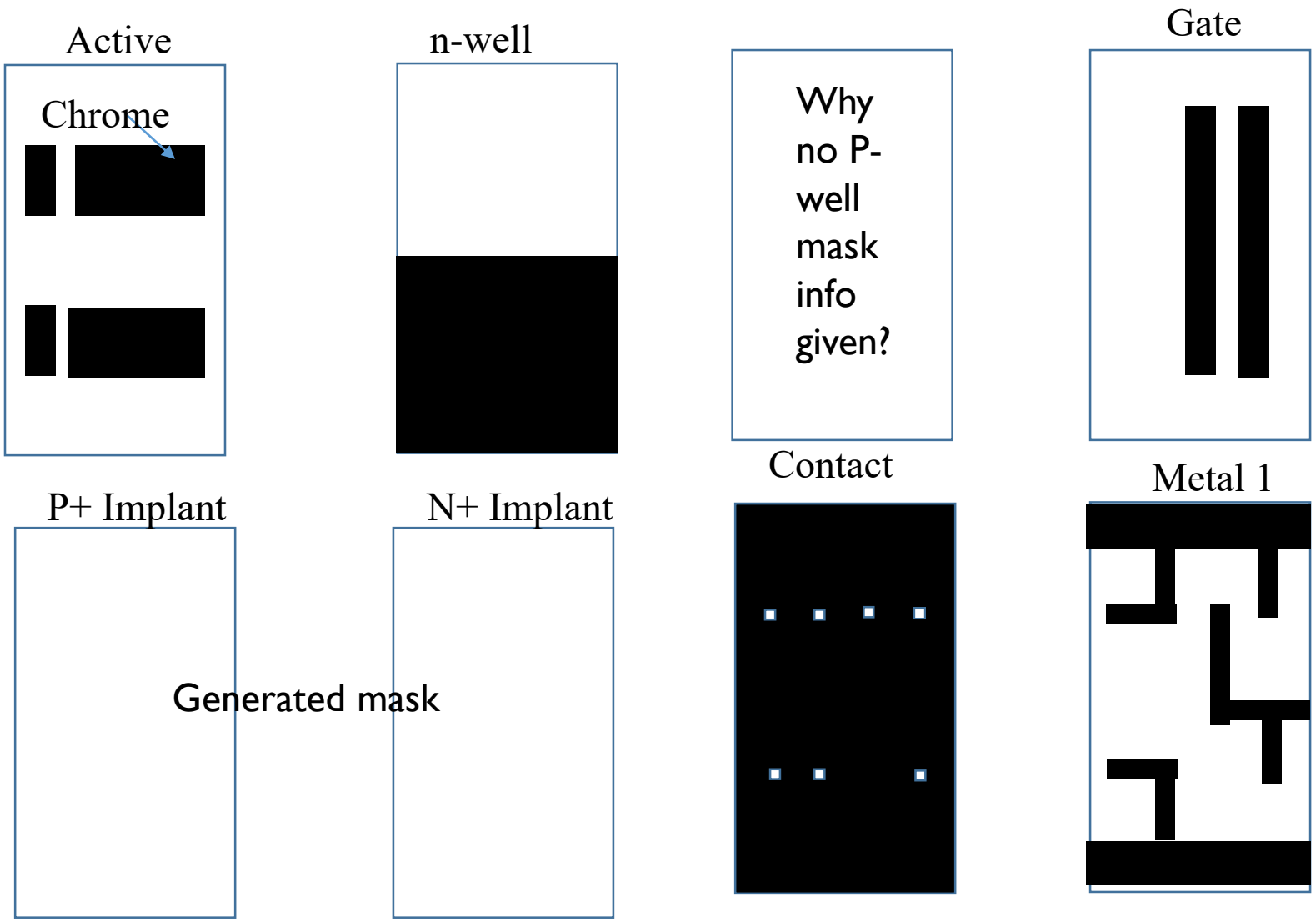
p-well



Can you draw process cross section cut?

GDSII File: Standard Database Exchange

IC layout (Design) to Manufacuing foundry

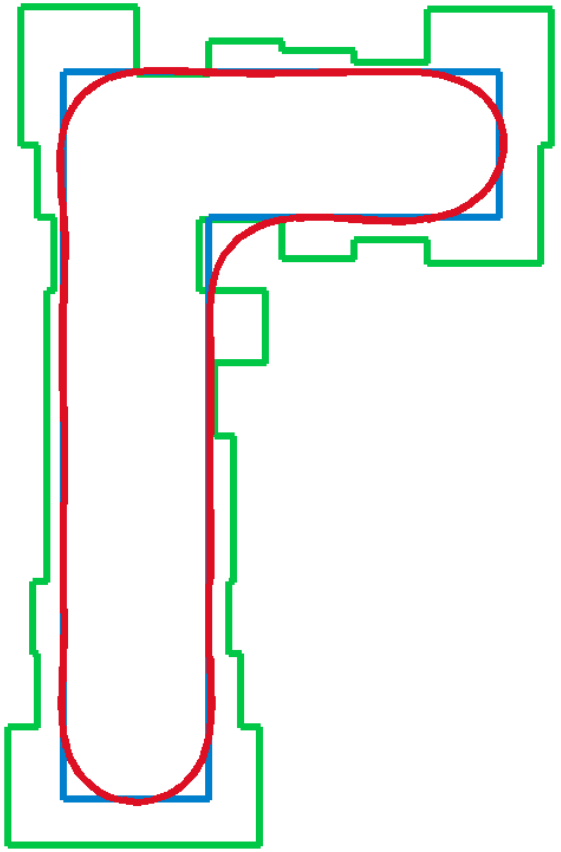


GDSII

- De facto industry standard
- Database file format
- Data base can “reconstruct” all mask infomation needed to fabricate a chip
  - i.e fabricate photomask
- File Fabless company (Apple, Qualcom, AMD Nvidia, etc) transfers to Foundry (TSMC, Samsung, Intel, SMIC, GF, UMC)

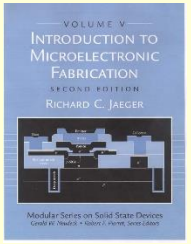
OPC: (Optical Proximity Correction)

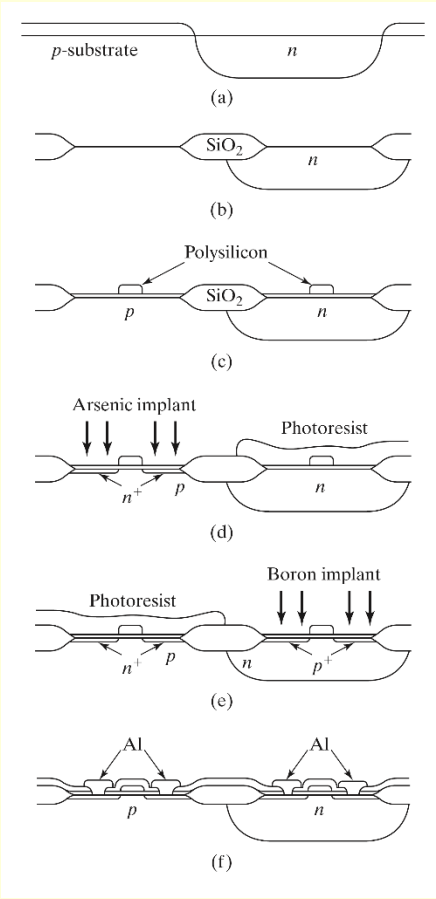
- De facto enhancement technique to compensate for image error due to diffraction
- Corners round due to
- Always difference between drawn actual features on wafer
- Draw different than mask feature



- Example: Gate endcap rounding and transistor L_E/leakage

CMOS Technology
N-Well Technology Cross-Section





Oxidation

Photolithography

Implantation

Diffusion

Etching

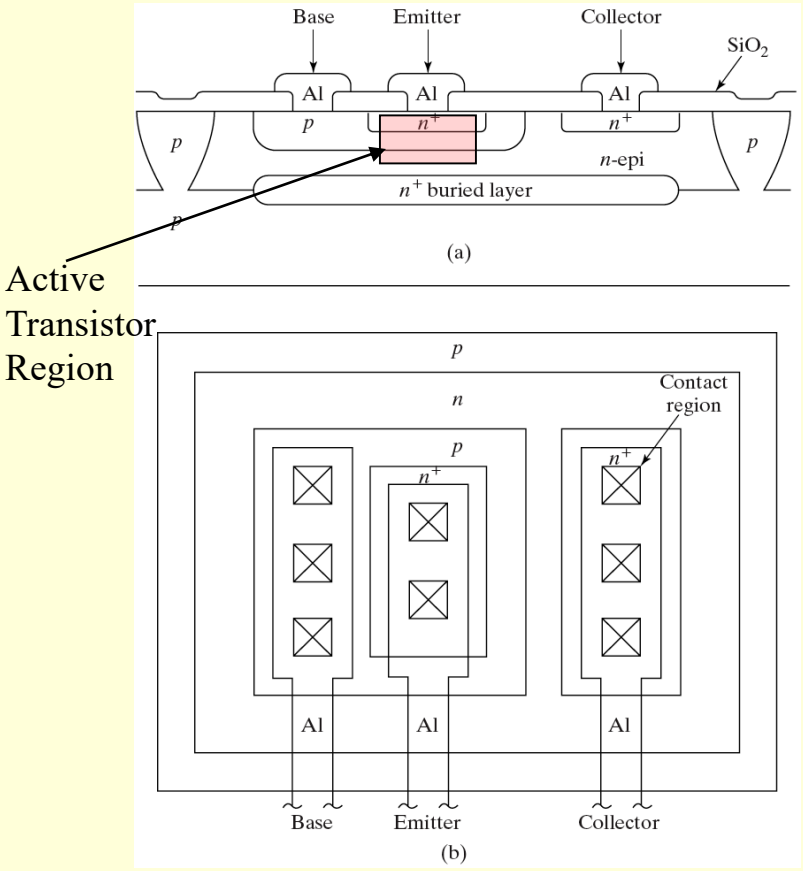
Film Deposition

- Complementary Metal-Oxide Semiconductor Technology
- Dominant Technology in Integrated Circuits Today!
- Requires both NMOS and PMOS Transistors

FIGURE 1.8

Cross-sectional views at major steps in a basic CMOS process. (a) Following *n*-well diffusion, (b) following selective oxidation, and (c) following gate oxidation and polysilicon gate definition; (d) NMOS source/drain implantation; (e) PMOS source/drain implantation; (f) structure following contact and metal mask steps.

Bipolar Transistor
Top View and Cross-Section

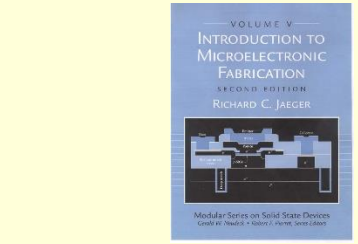


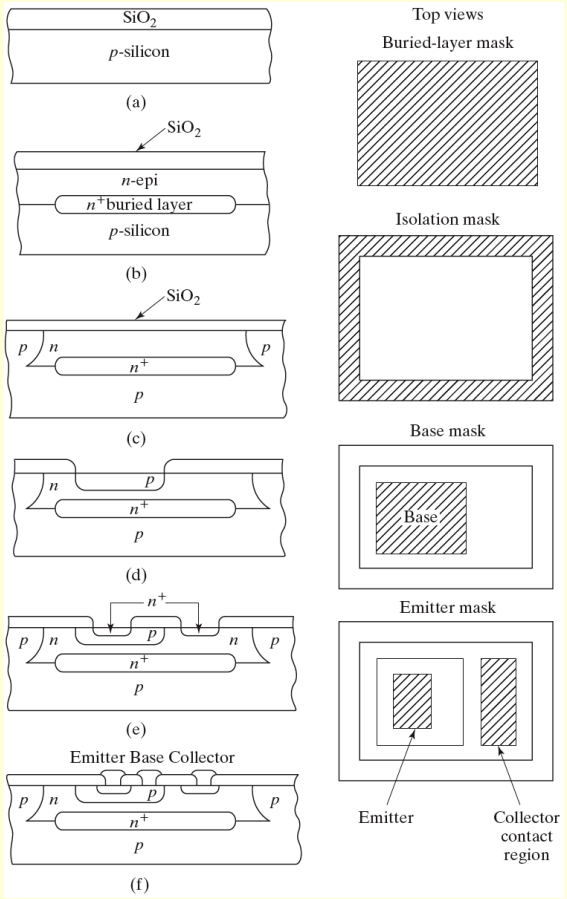
- Bipolar Junction Transistor (BJT)
- Standard Buried Collector Process (SBC)
- n- and p-type semiconductor regions
- Thick and thin oxides
- Etching Openings
- Metal (Al) Interconnections

FIGURE 1.5

The basic structure of a junction-isolated bipolar transistor. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a).

SBC Process
Key Steps

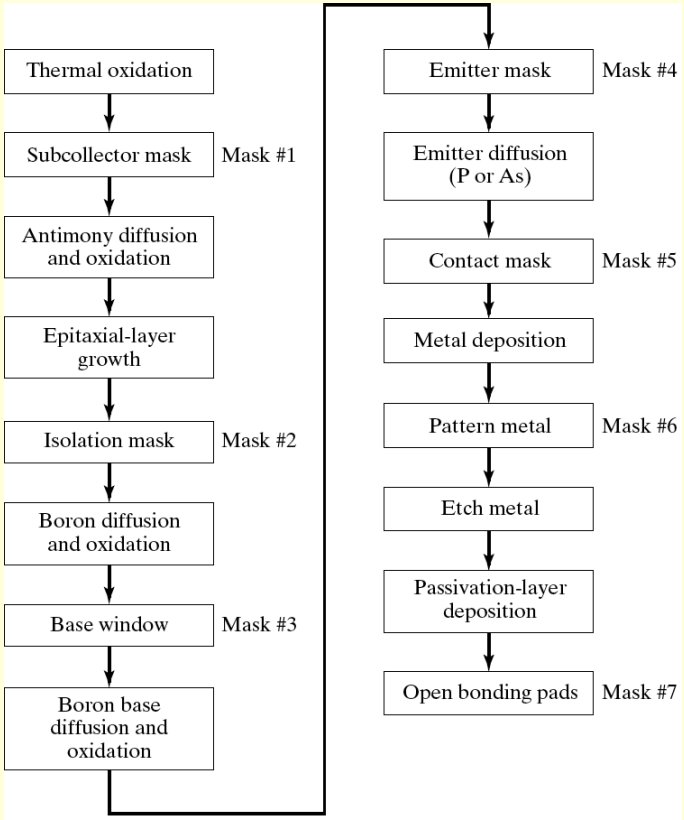




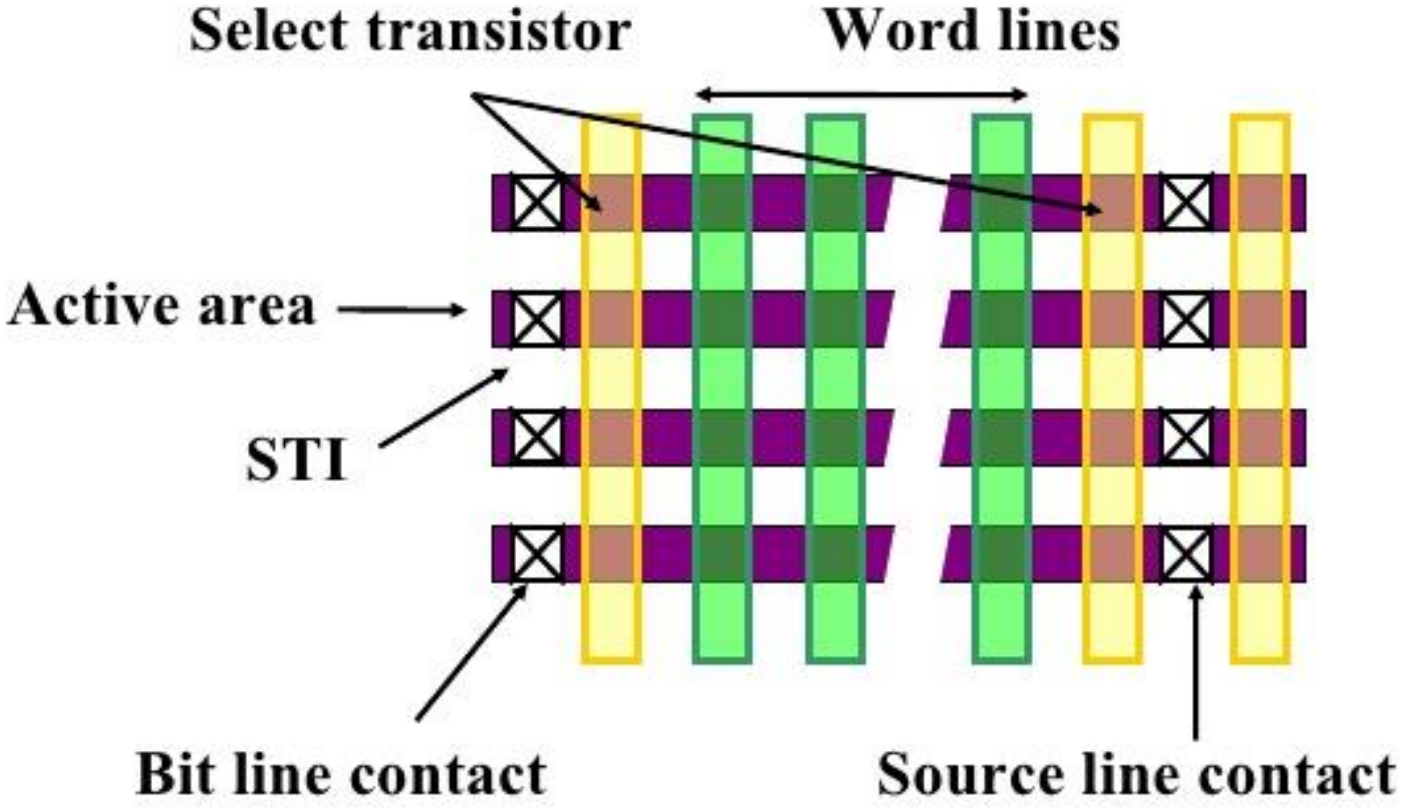
- Oxidation
- Photolithography
- Implantation
- Diffusion
- Etching
- Film Deposition

FIGURE 1.9

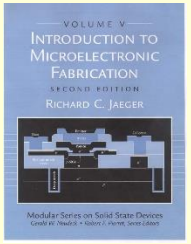
Cross-sectional view of the major steps in a basic bipolar process. (a) Wafer with silicon dioxide layer; (b) following buried-layer diffusion using first mask, and subsequent epitaxial layer growth and oxidation; (c) following deep-isolation diffusion using second mask; (d) following boron-base diffusion using third mask; (e) fourth mask defines emitter and collector contact regions; (f) final structure following contact and metal mask steps.



NAND Flash Memory



References



[1] *Digest of the IEEE International Solid-State Circuit Conference*, held in February of each year. (http://www.sscs.org/isscc)

[2] *Digest of the IEEE International Electron Devices Meeting*, held in December of each year. (http://www.ieee.org/conference/iedm)

[3] *Digests of the International VLSI Technology and Circuits Symposia*, co-sponsored by the IEEE and JSAP, held in June of each year. (http://www.vlsisymposium.org)

[4] *The International Technology Roadmap for Semiconductors*, The Semiconductor Industry Association (SIA), San Jose, CA, 1999. (http://www.semichips.org)

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End of Chapter 1

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